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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,384	AUGSBURG ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,16-23 and 31-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,16-18,20-23,31,32,34-36 and 38-40* is/are rejected.

7)☒ Claim(s) *4,19,33 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 16-23, and 31-40 have been considered. Claims 1-8, 16-19 and 22-23 have been amended as per Applicant's request. Claims 8-15 and 24-30 have been cancelled as per Applicant's request. New claims 31-40 have been added as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as filed 13 March 2007 and Amendment as field 13 March 2007.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 13 March 2007 has been entered.

Allowable Subject Matter

4. Claims 4, 19, 33, and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: Claims 4, 19, 33, and 37 specifically recite that the threshold value is 50%. Most prior art searched and found have taught that the possibility of a data dependency is either 100%, i.e. that a data dependency definitely exists, or 0%, i.e. that a data dependency definitely does not exist. None of the prior art has taught that the threshold value being tested is between 0% and 100%,

i.e. that the data dependency is 100% certain or 0% certain. The small amounts of prior art that did discuss finding confidence values did not discuss these values being definitive, quantitative values, such as percentages, but that they are possibilities with more qualitative values, such as stronger to weaker likelihoods.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 3, 16, 17, 18, 21, 34, 35, and 36 are rejected under 35 U.S.C. 102(b) as being taught by Ito et al., U.S. Patent Number 5,742,782 (herein referred to as Ito).

8. Referring to claims 1, 16, and 34, taking claim 16 as exemplary, Ito has taught a simultaneous multithreaded computer processor with speculative instruction issue that increases throughput, the computer processor comprising:

a. Multiple independent input buffers, wherein one set of buffers is provided for each of a plurality of independent threads of instructions (Ito column 5, lines 36-41 "When it is desired to process 3 instruction streams or threads...the instruction decoder **23** is made up of 3 instruction decoder parts..."; column 7, lines 1-11 "...an embodiment of the instruction decoder **23** which includes an instruction buffer **31**..."; and Figure 2);

b. Instruction issue logic that has an output buffer (Ito column 10, lines 13-21 "...each instruction decoder **23** until schedule buffer **37** sends it to the execution

part **25**..." and Figure 3) and is connected to the independent input buffers (Ito column 10, lines 13-21 "...each instruction decoder **23** until schedule buffer **37** sends it to the execution part **25**..." and Figure 3), wherein the instruction issue logic:

i. Receives a set of instructions comprising one instruction from each of the threads of instructions (Ito column 5, lines 36-61 "When it is desired to process 3 instruction streams or threads...the threads A, B and C sent..." and Figure 1, elements 23a-d and 24a-d – In regards to Ito, the instruction decoder and instruction scheduler acts as an issue unit since, together, they determine which instructions are to be issued to the instruction execution units from each thread.);

ii. Identifies as dependent instructions those received instructions that require a result from a prerequisite instruction (Ito column 7, line 35 to column 8, line 20 "...Explanation will first be made as the above 3 sorts of data dependent relationships...");

iii. Determines a probability for each instruction that the instruction will complete all stages of a multi-stage instruction pipeline of the processor without causing a stall (Ito column 5, lines 42-54 "The instruction decoder **23** acts (1) to judge the possibility of issuing an operation instructions..."; column 7, line 1 to column 8, line 20 "The operation of the instruction decoder **23**...includes an instruction buffer **31**, a competition judger **32**, a dependent relationship resolver **33**..."; Figure 1; Figure 2; Figure 10; and

Figure 11 – In regards to Ito, the decoder determines whether the instruction will possibly stall by determining whether there is a resource conflict with the competition judger, which would necessitate a delay to wait for a resource to be freed for use, and whether there is a data dependency with the data relationship resolver, which requires a delay to ensure that the data is available. When either of these possibilities occurs, i.e. these possibilities have a 100% probability of occurring, the instruction is not selected for issue. However, when neither of these possibilities occur, i.e. the instruction has a 100% probability of not stalling due to these condition, the instruction is issued.);

iv. Selects the received instruction of the set that is least likely to cause a stall in the multi-stage pipeline (Ito column 5, lines 42-54 "The instruction decoder **23** acts (1) to judge the possibility of issuing an operation instructions..."; column 7, line 1 to column 8, line 20 "The operation of the instruction decoder **23**...includes an instruction buffer **31**, a competition judger **32**, a dependent relationship resolver **33**..."; Figure 1; Figure 2; Figure 10; and Figure 11 – In regards to Ito, when it is determined that neither of a resource competition or data dependency has occurred, i.e. the instruction has a 100% probability of not stalling due to these condition, the instruction is issued to the execution units.); and

v. Issues the selected instruction into the pipeline for processing, from the instruction issue logic (Ito column 6, lines 5-20 "...The execution part **25**.

which is arranged on an operational pipeline basis..." and Figure 1, elements 25a-d), when the probability for the selected instruction is above a predetermined threshold (Ito column 5, lines 42-54 "The instruction decoder **23** acts (1) to judge the possibility of issuing an operation instructions..."; column 7, line 1 to column 8, line 20 "The operation of the instruction decoder **23**...includes an instruction buffer **31**, a competition judger **32**, a dependent relationship resolver **33**..."; Figure 1; Figure 2; Figure 10; and Figure 11 – In regards to Ito, when it is determined that neither of a resource competition or data dependency has occurred, i.e. the instruction has a 100% probability of not stalling due to these condition, the instruction is issued to the execution units.); and

c. Wherein a first stage of the multi-stage pipeline is connected to an output buffer of the instruction issue logic (Ito column 10, lines 13-21 "...each instruction decoder **23** until schedule buffer **37** sends it to the execution part **25**..." and Figure 3).

9. Claims 1 and 34 have similar limitations to claim 16 and are rejected for similar reasons. The only difference between claim 1 and claim 16 is that claim 1 is for a method instead of a computer processor. The only difference between claim 34 and claim 16 is that claim 34 is for a computer program product instead of a computer processor.

10. Referring to claims 2, 17, and 35, taking claim 16 as exemplary, Ito has taught the computer processor of claim 16, wherein the instruction issue logic determines whether there is a shared resource conflict between two or more of the received instructions (Ito column 7, line 35

to column 8, line 20 "...Explanation will first be made as the above 3 sorts of data dependent relationships...").

11. Claims 2 and 35 have similar limitations to claim 17 and are rejected for similar reasons. The only difference between claim 2 and claim 17 is that claim 2 is for a method instead of a computer processor. The only difference between claim 35 and claim 17 is that claim 35 is for a computer program product instead of a computer processor.

12. Referring to claims 3, 18, and 36, taking claim 18 as exemplary, Ito has taught the computer processor of claim 16, wherein the instruction issue logic resolves a given one of said shared resource conflicts, between two or more of said received instructions, after said given conflict has been discovered (Ito column 7, line 35 to column 8, line 20 "...Explanation will first be made as the above 3 sorts of data dependent relationships...").

13. Claims 3 and 36 have similar limitations to claim 18 and are rejected for similar reasons. The only difference between claim 3 and claim 18 is that claim 3 is for a method instead of a computer processor. The only difference between claim 36 and claim 18 is that claim 36 is for a computer program product instead of a computer processor.

14. Referring to claim 21, Ito has taught the computer processor of claim 16, wherein the instruction issue logic further identifies as dependent instructions those received instructions that have a conflict over a shared resource within a computer system in which the computer processor operates (Ito column 5, lines 42-54 "The instruction decoder **23** acts (1) to judge the possibility of issuing an operation instructions..."; column 7, line 1 to column 8, line 20 "The operation of the instruction decoder **23**...includes an instruction buffer **31**, a competition judger **32**, a dependent relationship resolver **33**..."; Figure 1; Figure 2; Figure 10; and Figure 11).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 5-7, 19-20, 22-23, and 38-40 rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al., U.S. Patent Number 5,742,782 (herein referred to as Ito) as applied to claims 1, 16, 21, and 34 above, and further in view of Hinton, U.S. Patent Number 5,555,432 (herein referred to as Hinton).

17. Referring to claims 5, 20, and 38, taking claim 20 as exemplary, Ito has not explicitly taught the computer processor of claim 16, wherein instruction issue logic predicts a stage, within the multi-stage instruction pipeline, where results of each instruction will be available, and determines the probability for a dependent instruction by calculating a critical distance comprising the number of stages between a stage when the dependent instruction will need a given result, and the stage when the result will be available. However, Ito has taught that an instruction held in the decoder due to a data dependency is issued and executed when the data dependency is resolved, but not exactly how and when the data dependent instruction is issued and executed. Hinton has taught when to issue and execute data dependent instructions, specifically, Hinton has taught the computer processor of claim 16, wherein instruction issue logic predicts a stage, within the multi-stage instruction pipeline, where results of each instruction will be available, and determines the probability for a dependent instruction by calculating a critical distance comprising the number of stages between a stage when the

dependent instruction will need a given result, and the stage when the result will be available (Hinton column 3, lines 31-53 "...The execution resource indicates future availability to receive additional instructions a number of clock cycles prior to completions..."; column 7, lines 34-50 "...The execution unit **107** sends the two clock preliminary valid signal by predicting the completion of executing instructions (and ensuing write-back of the execution result) during each clock cycle..."; and Figure 2). A person of ordinary skill in the art at the time the invention was made, and as taught by Hinton, would have recognized that predicting when the results will be available for a data dependent instruction and starting execution of the dependent instruction accordingly reduces the idle time of the resources and improves throughput performance (Hinton column 2, lines 33-42 "...Such idle time reduces the instruction throughput performance..."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the prediction and issuance of Hinton in the device of Ito to improve throughput performance.

18. Claims 5 and 38 have similar limitations to claim 20 and are rejected for similar reasons. The only difference between claim 5 and claim 20 is that claim 5 is for a method instead of a computer processor. The only difference between claim 38 and claim 20 is that claim 38 is for a computer program product instead of a computer processor.

19. Referring to claims 6, 22, and 39, taking claim 22 as exemplary, Ito in view of Hinton has taught the computer processor of claim 21, wherein the probability for a dependent instruction is determined based upon a current location and the predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict (Hinton column 3, lines 31-53 "...The execution resource indicates future availability to receive additional

instructions a number of clock cycles prior to completions..."; column 7, lines 34-50 "...The execution unit **107** sends the two clock preliminary valid signal by predicting the completion of executing instructions (and ensuing write-back of the execution result) during each clock cycle..."; and Figure 2).

20. Claims 6 and 39 have similar limitations to claim 22 and are rejected for similar reasons. The only difference between claim 6 and claim 22 is that claim 6 is for a method instead of a computer processor. The only difference between claim 39 and claim 22 is that claim 39 is for a computer program product instead of a computer processor.

21. Referring to claims 7, 23, and 40, taking claim 7 as exemplary, Ito in view of Hinton has taught The computer processor of claims 22, wherein the instruction issue logic dynamically recalculates the probability for each instruction based on a current contents of the pipeline and a current status of any shared resources (Ito column 5, lines 42-54 "The instruction decoder **23** acts (1) to judge the possibility of issuing an operation instructions..."; column 7, line 1 to column 8, line 20 "The operation of the instruction decoder **23**...includes an instruction buffer **31**, a competition judger **32**, a dependent relationship resolver **33**..."; Figure 1; Figure 2; Figure 10; and Figure 11 – In regards to Ito, the competition judger and dependent relationship resolver is updated with the available resources each machine cycle.).

22. Claims 7 and 40 have similar limitations to claim 23 and are rejected for similar reasons. The only difference between claim 7 and claim 23 is that claim 7 is for a method instead of a computer processor. The only difference between claim 40 and claim 23 is that claim 40 is for a computer program product instead of a computer processor.

23. Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al., U.S. Patent Number 5,742,782 (herein referred to as Ito) as applied to claims 1, 16, 21, and 34 above, and further in view of Hinton, U.S. Patent Number 5,555,432 (herein referred to as Hinton).

24. Referring to claim 31, Ito has taught a method for issuing instructions in a multithreaded computer processor, comprising the steps of:

a. Receiving a set of computer instructions in an instruction issue logic, wherein each set of instructions comprises one instruction from each of a plurality of independent instruction threads (Ito column 5, lines 36-61 "When it is desired to process 3 instruction streams or threads...the threads A, B and C sent..." and Figure 1, elements 23a-d and 24a-d – In regards to Ito, the instruction decoder and instruction scheduler acts as an issue unit since, together, they determine which instructions are to be issued to the instruction execution units from each thread.);

b. Identifying as dependent instructions those received instructions that require a result from a prerequisite instruction (Ito column 7, line 35 to column 8, line 20 "...Explanation will first be made as the above 3 sorts of data dependent relationships...");

c. Determining a probability that the selected instruction will complete all stages of the pipeline without causing a stall (Ito column 5, lines 42-54 "The instruction decoder **23** acts (1) to judge the possibility of issuing an operation instructions..."; column 7, line 1 to column 8, line 20 "The operation of the instruction decoder **23**...includes an instruction buffer **31**, a competition judger

32, a dependent relationship resolver **33**..."; Figure 1; Figure 2; Figure 10; and Figure 11 – In regards to Ito, the decoder determines whether the instruction will possibly stall by determining whether there is a resource conflict with the competition judger, which would necessitate a delay to wait for a resource to be freed for use, and whether there is a data dependency with the data relationship resolver, which requires a delay to ensure that the data is available. When either of these possibilities occurs, i.e. these possibilities have a 100% probability of occurring, the instruction is not selected for issue. However, when neither of these possibilities occur, i.e. the instruction has a 100% probability of not stalling due to these condition, the instruction is issued.)

d. Issuing the selected instruction into the pipeline for processing, from the instruction issue logic (Ito column 6, lines 5-20 "...The execution part **25**. which is arranged on an operational pipeline basis..." and Figure 1, elements 25a-d), when the probability is above a predetermined threshold (Ito column 5, lines 42-54 "The instruction decoder **23** acts (1) to judge the possibility of issuing an operation instructions..."; column 7, line 1 to column 8, line 20 "The operation of the instruction decoder **23**...includes an instruction buffer **31**, a competition judger **32**, a dependent relationship resolver **33**..."; Figure 1; Figure 2; Figure 10; and Figure 11 – In regards to Ito, when it is determined that neither of a resource competition or data dependency has occurred, i.e. the instruction has a 100% probability of not stalling due to these condition, the instruction is issued to the execution units.).

25. Ito has not explicitly taught

a. Predicting a stage, within a multi-stage instruction pipeline of the computer processor, where results of each instruction will be available;

b. Calculating a critical distance comprising the number of stages between a stage when a selected dependent instruction will need a given result, and the stage when the result will be available; and

c. Determining whether the selected instruction is within the critical distance.

26. However, Ito has taught that an instruction held in the decoder due to a data dependency is issued and executed when the data dependency is resolved, but not exactly how and when the data dependent instruction is issued and executed. Hinton has taught when to issue and execute data dependent instructions, specifically, Hinton has taught

a. Predicting a stage, within a multi-stage instruction pipeline of the computer processor, where results of each instruction will be available (Hinton column 3, lines 31-53 "...The execution resource indicates future availability to receive additional instructions a number of clock cycles prior to completions..."; column 7, lines 34-50 "...The execution unit **107** sends the two clock preliminary valid signal by predicting the completion of executing instructions (and ensuing write-back of the execution result) during each clock cycle..."; and Figure 2);

b. Calculating a critical distance comprising the number of stages between a stage when a selected dependent instruction will need a given result, and the stage when the result will be available (Hinton column 3, lines 31-53 "...The execution resource indicates future availability to receive additional instructions a number of

clock cycles prior to completions..."; column 7, lines 34-50 "...The execution unit **107** sends the two clock preliminary valid signal by predicting the completion of executing instructions (and ensuing write-back of the execution result) during each clock cycle..."; and Figure 2); and

c. Determining whether the selected instruction is within the critical distance (Hinton column 3, lines 31-53 "...The execution resource indicates future availability to receive additional instructions a number of clock cycles prior to completions..."; column 7, lines 34-50 "...The execution unit **107** sends the two clock preliminary valid signal by predicting the completion of executing instructions (and ensuing write-back of the execution result) during each clock cycle..."; and Figure 2).

27. A person of ordinary skill in the art at the time the invention was made, and as taught by Hinton, would have recognized that predicting when the results will be available for a data dependent instruction and starting execution of the dependent instruction accordingly reduces the idle time of the resources and improves throughput performance (Hinton column 2, lines 33-42 "...Such idle time reduces the instruction throughput performance..."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the prediction and issuance of Hinton in the device of Ito to improve throughput performance.

28. Referring to claim 32, Ito in view of Hinton has taught the method of claim 3 1, wherein said probability is expressed as a percentage value (Ito column 6, lines 5-20 "...The execution part **25**. which is arranged on an operational pipeline basis..." and Figure 1, elements 25a-d),

when the probability is above a predetermined threshold (Ito column 5, lines 42-54 "The instruction decoder **23** acts (1) to judge the possibility of issuing an operation instructions..."; column 7, line 1 to column 8, line 20 "The operation of the instruction decoder **23**...includes an instruction buffer **31**, a competition judger **32**, a dependent relationship resolver **33**..."; Figure 1; Figure 2; Figure 10; and Figure 11 – In regards to Ito, when it is determined that neither of a resource competition or data dependency has occurred, i.e. the instruction has a 100% probability of not stalling due to these condition, the instruction is issued to the execution units. Also, the representation of the data, whether in percentages, Boolean, or binary is irrelevant, since the functionality and affects are the same.).

Response to Arguments

29. Applicant's arguments with respect to claims 1-7, 16-23, and 31-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Chung et al., U.S. Patent Number 5,404,469, has taught static interleave scheduling of multiple threads for execution simultaneously.

b. Keckler et al., U.S. Patent Number 5,574,939, has taught dynamically scheduling threads for execution simultaneously with one of the criteria being whether the instruction being scheduled has is a data dependent instruction on a still in-process instruction.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J Li
Examiner
Art Unit 2183

28 March 2007